IMPROVING PERFORMANCE OF SURGE PROTECTION CIRCUITS WITH CURRENT LIMITING DEVICES

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TABLE OF CONTENTS

ABSTRACT

This Application Note presents the benefits of using CALY Technologies' flagship, the Current Limiting Device (CLD), for ESD, surge and lightning protection.

A case study is presented where a CLD is used in a π (Pi-type) protection circuit against surge and lightning, and how this improves the overall performance of the protection and increases reliability (lifetime) of the voltage clamping devices. As the presented example considers the implementation of a lightning protection of industrial communication lines (RS-422/485, 4-20mA, Ethernet, audio/video), typical 1.2/50µs-8/20µs waveforms have been chosen to illustrate this example.

In this case-study, it is pointed out how the CLD improves the clamping capabilities and reduces stress on the clamping device, while decreasing DC or AC losses of the circuit. As a result, the overall circuit performance is improved and the total circuit footprint can be strongly reduced.

This Application Note is aimed at customers designing and deploying CLD-based lightning and surge protection applications, by providing an application schematic for audio/video, data and communication protection circuits.

SURGE PROTECTION CONTEXT

ESD and lightning events require appropriate topologies to ensure an accurate circuit protection. Surge levels, pulse time duration and wave shapes are defined in several standards covering large application fields, from Automotive to RF front-ends. Among the most popular, IEC 61000-4-2, IEC 61000-4-5, RTCA/DO-160 section 22, Telcordia GR-1089-CORE can be cited. Pulse amplitude levels can reach few thousand Volts or Amps, while durations can go up to several milliseconds.

For voltage surges, a first-level protection circuit can be made with non-linear devices –transient voltage suppressors (TVS), varistors (MOV) – acting as voltage clamping element (see Figure 1). However, such devices are not designed to either react fast enough (varistors) or to sustain the large power levels dissipated (TVS) during ESD and lightning events.

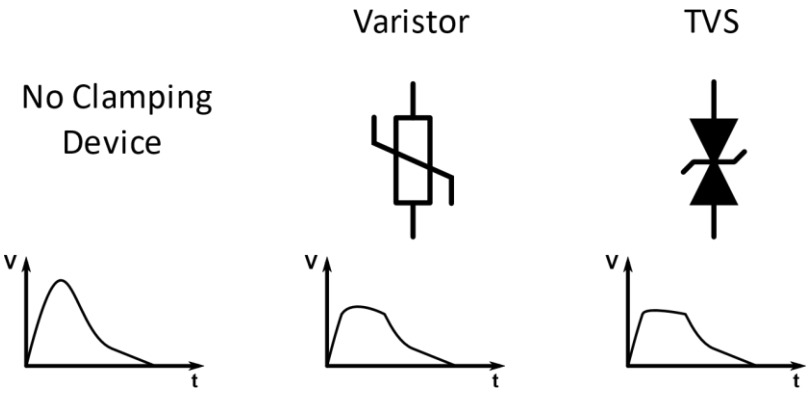

Figure 1: Usual clamping devices used in protection circuits

Usually, TVS offer a sharper and quicker voltage clamping than varistors. This is due to their lower dynamic resistance as well as parasitic capacitance. Conversely, varistors allow higher dissipated power levels than TVS. The reason why varistors usually sustain higher energies than TVS for the same die volume mainly depends on which type of semiconductor is used.

One major drawback of varistors is their failure mode. Indeed, they commonly fail in a short circuit mode when subjected to a voltage close to their clamping voltage for an extended period. As a result, this failure induces a high inrush current that must be tackled with a fuse or other type of breaking circuit.

To benefit from the TVS advantages (fast response time and excellent clamping accuracy) while withstanding high dissipated power levels, several TVS must be paralleled in order to distribute the pulse energy. Even if a satisfactory operation can be achieved, this is a costly and bulky solution. It also implies that all paralleled devices must be closely matched, and that must be ensured by accurate screening.

Because of their characteristics, TVS are the most appropriate devices to clamp voltages as they offer a behavior close to ideal “voltage references”, provided it is properly biased during a surge event. As a result, during a voltage surge they should operate at power levels under their maximum ratings. This approach will be discussed and detailed in the following sections.

"ASSISTED" TVS PROTECTION

There are two ways to lessen the dissipated energy in the clamping device:

- By decreasing the peak power level
- By reducing the conduction time of this device.

These two possibilities result in different device associations. Figure 2 depicts these two circuits.

Decreasing the peak power level implies a lower voltage across the TVS. In this case, the TVS could be paralleled with a varistor. The varistor should have the same or a slightly lower voltage rating than the TVS. That way, the varistor's soft clipping voltage helps balancing the induced surge current between the varistor and the TVS, thus reducing the power dissipated by this latter. Care must be taken when selecting the varistor voltage/power rating, required to reach the optimum current distribution between the varistor and the TVS. This topology is called varistor-assisted TVS.

If the alternative of decreasing the conduction time of the TVS is preferred, a triggering device can be added in parallel with the TVS. This additional device must short the voltage across the TVS as soon as possible (few µs in general) when a surge occurs. Practically, for this task either active circuits can be used, such as crowbar/foldback circuits with thyristors, or passive devices like gas discharge tubes (GDT).

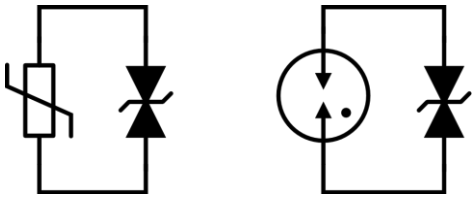

Figure 2: Varistor-assisted TVS (left) and GDT-assisted TVS (right).

In both cases presented here above and depicted in Figure 2, an issue remains: the TVS is not well protected against over-currents occurring on heavy surges, even if the varistor has a voltage rating close to that of the TVS or if the gas discharge tube triggers very quickly.

As a conclusion, a device ensuring appropriate TVS biasing during surges would provide the solution to overcome this problem.

PROPERLY BIASING THE TVS: THE Π PROTECTION CIRCUIT

In the following, the GDT-assisted TVS case is considered. Figure 3 depicts the typical GDT behavior when subjected to voltage surges.

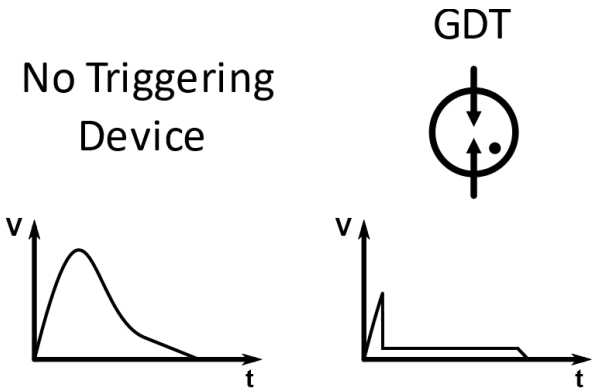

Figure 3: Typical GDT waveform

At the beginning of a surge event, the GDT is unable to trigger during first few micro-seconds because the internal ignition process takes some time to be set. During this stage, the surge voltage is directly applied to the TVS and no current limitation occurs. This can lead to very high dissipated power in the TVS. When the GDT is triggered, the TVS voltage is reduced to the GDT arc voltage, so that no more power is dissipated in the TVS.

To prevent from large dissipated power levels in the TVS, a resistor is generally used in series with it, which gives the well-known π protection circuit (Figure 4).

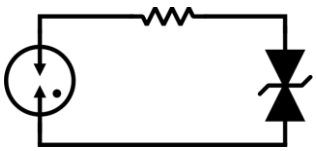

Figure 4: The π protection circuit

Figure 5 shows the typical waveforms and conduction phases when a surge is applied to the circuit (with output in open-circuit).

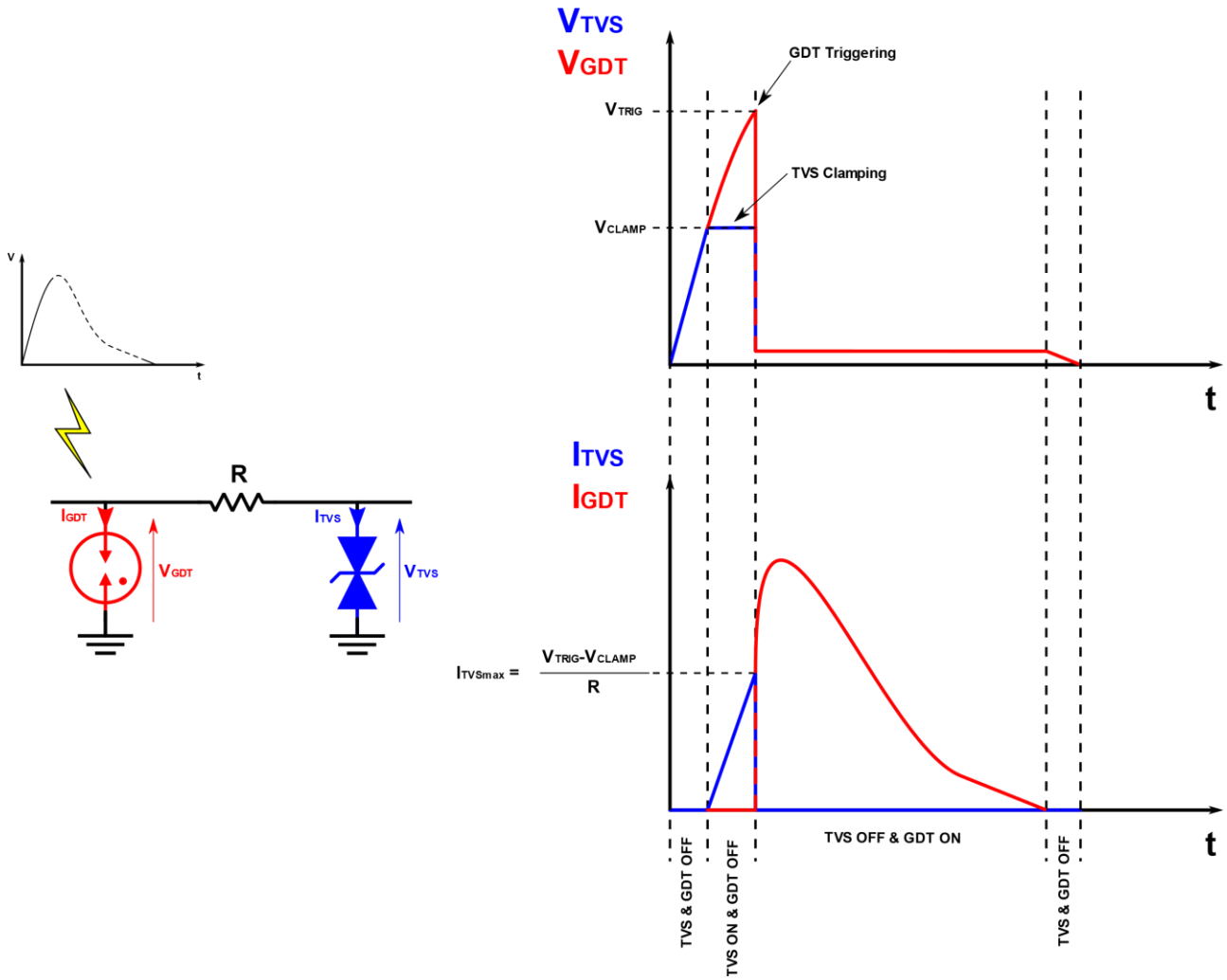

Figure 5: Typical waveforms and conduction phases in the π protection circuit during a surge event.

Whereas the TVS clamping level is constant with voltage or dV/dt, the GDT triggering voltage varies, especially with dV/dt. By the way, this parameter is generally specified in GDT datasheets according to different voltage slew rates. This variation tends to alter the GDT ignition time: the higher slew rate, the shorter GDT ignition time. This point will be highlighted with measurements below.

The main drawback of this association is precisely this series resistor. Indeed, if the protection circuit is used on a power supply rail, the resistance must be as low as possible to limit losses and voltage drops. If it is used on a communication line, it must also be low and non-inductive because it induces AC losses with TVS parasitics (RLC low-pass filter).

On the other hand, this resistor must be large enough to limit the current in the TVS to appropriate values. Thus, a trade-off must be made concerning the resistor value.

The CLD can address this issue because it acts as a non-linear resistor. All the benefits will be described in detail in the next section.

LOOKING FOR LOW INSERTION LOSSES? THE BENEFITS OF THE CLD

It has been shown above that a TVS can be considered as a quasi-ideal voltage reference: that is a voltage source, when in clamping operation and at a constant current. Given the Kirchhoff's laws, the best way to do this is to associate a TVS with a current limiting device. This is also the right way to achieve the sharpest voltage clamping behavior.

Practically, the CLD acts as a current source with a low ON-state resistance value below the saturation current. When in saturation state, the current through the CLD, I_{SAT}, is almost independent of the voltage across it. Thus, the equivalent resistance of the device presents a non-linear behavior, increasing as voltage applied increases. Figure 6 depicts the typical IV characteristic of a CLD.

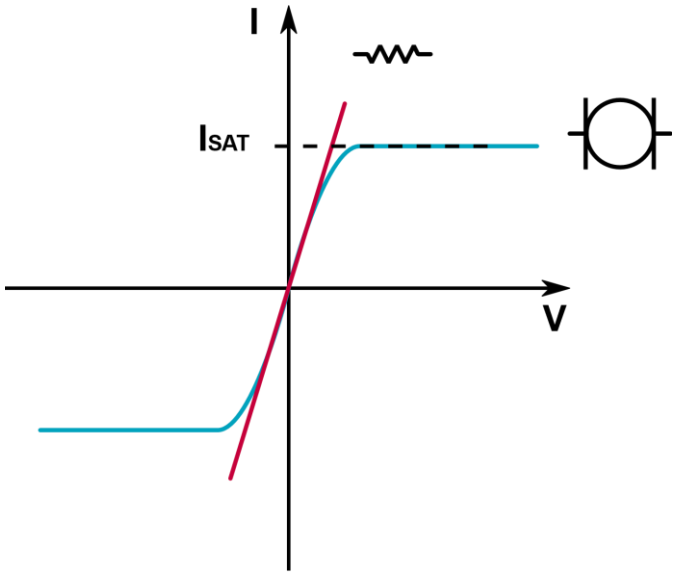

Figure 6: Typical IV characteristic for a CLD (blue line) and a resistor (red line)

As a result, when replacing the resistor in the π protection circuit, the CLD reduces losses and ensures a strong current limitation in the TVS, thus resulting in an excellent voltage clamping behavior. Figure 7 shows this improved version of the π protection circuit.

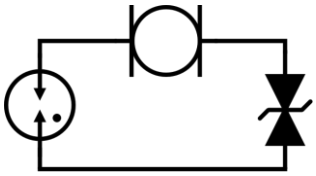

Figure 7: Improved version of the π protection circuit with the CLD

In the following section, the operation of this improved version is explained and experimental data is presented.

SOME EXPERIMENTAL RESULTS

Measurements have been carried out on the regular π protection circuit with resistor and with CLD. The measured configurations are shown in Figure 8. Current through devices is measured using low-resistance shunts.

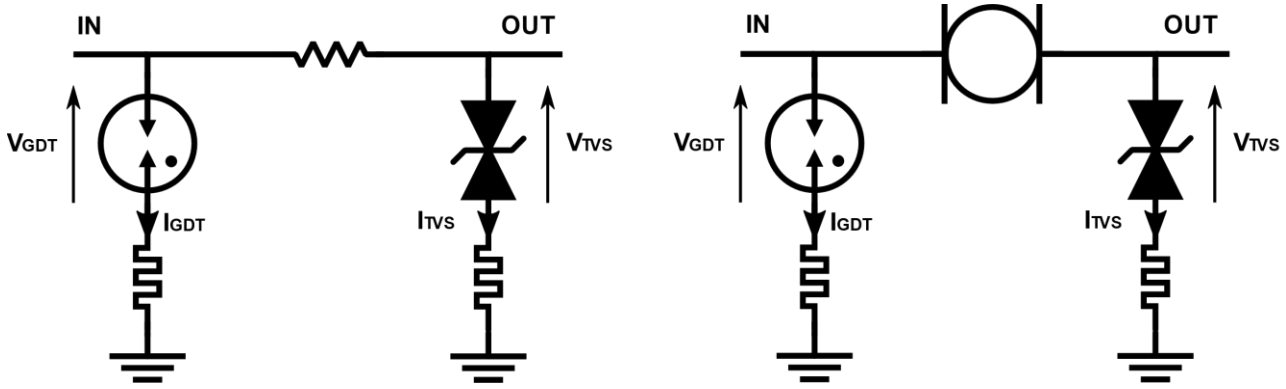

Figure 8: Measured configurations of the π protection circuit

The experimental setup is as follows:

- R=4.7Ω for the resistor version
- CALY KE12LS200T (R_{ON}=2Ω, I_{DSS}=4A) for the CLD version
- 90V GDT (DC Spark-over Voltage)
- 82V TVS (600W 10/1000µs)
- Shunt-measured current: 5mΩ for I_{GDT}, 200mΩ for I_{TVS}

Input surge waveforms were 1.2/50µs-8/20µs, with four voltage levels: 150V, 200V, 250V, 300V. Waveforms were generated using a Combination Wave Generator (Z_{INT}=2Ω).

Here below are the current waveforms through the TVS and the GDT (Figure 9) for resistive and CLD-based π protection circuits.

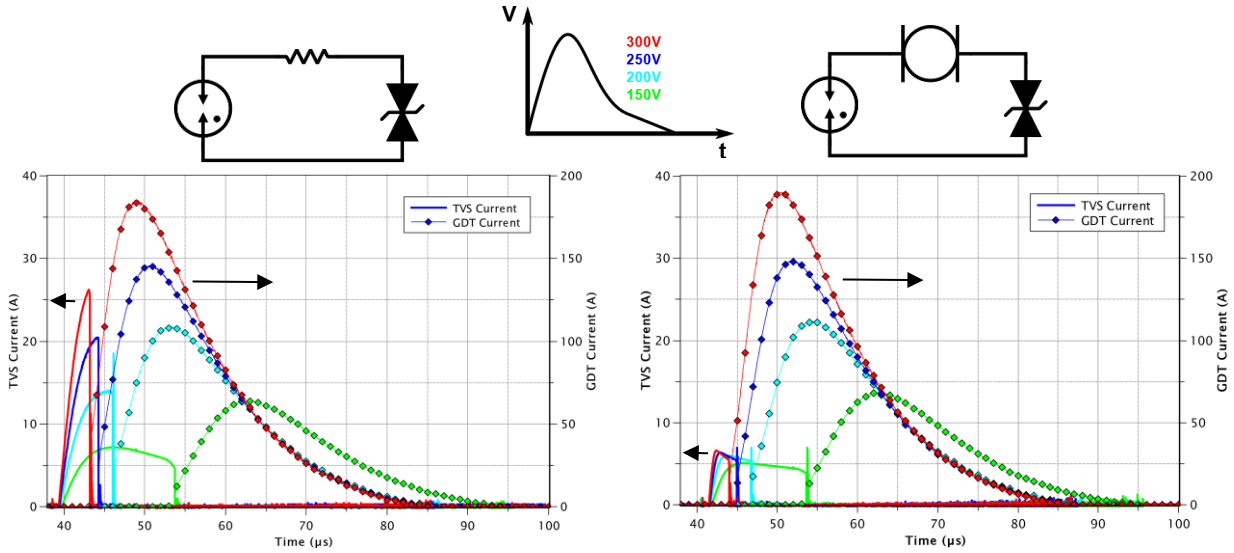

Figure 9: Current waveforms through GDT and TVS

Before the GDT ignition, the surge voltage appears across the resistor+TVS or CLD+TVS association. During this stage, the whole of the surge current flows through the TVS. Without CLD, this current is only determined by the voltage drop across the series resistor and the value of it. The higher the surge voltage, the higher the current through the TVS. In Figure 9 (left) the maximum current through the TVS reaches 26A.

With CLD instead of a resistor, the TVS current is kept constant at approximately 5A regardless of the voltage across the CLD+TVS association.

This current limitation also induces an excellent voltage clamping across the TVS as well as a bound dissipated power. This point is illustrated in Figure 10 and Figure 11.

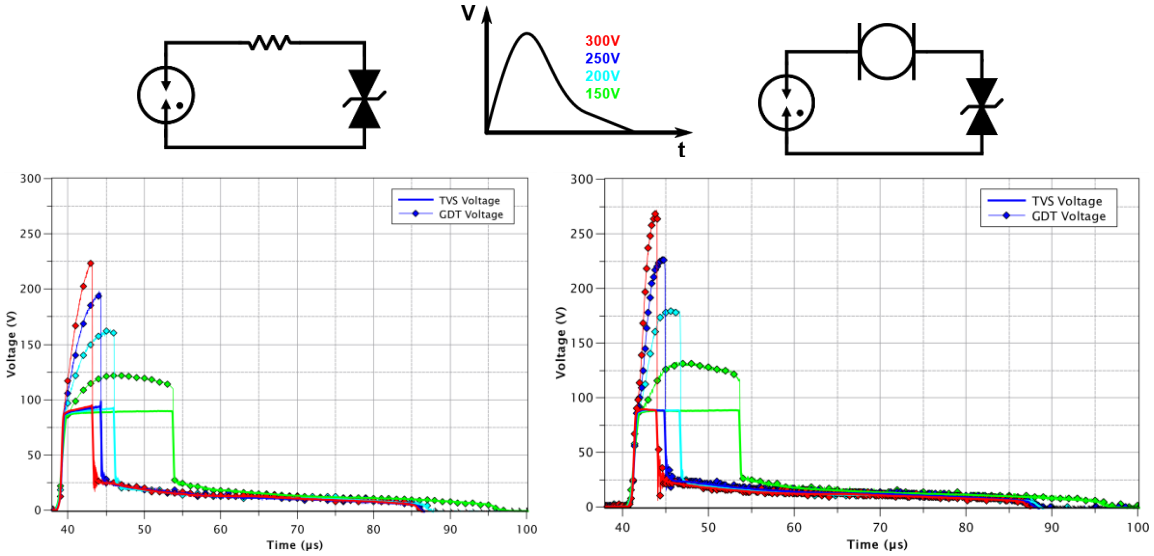

Figure 10: Voltage waveforms across GDT and TVS

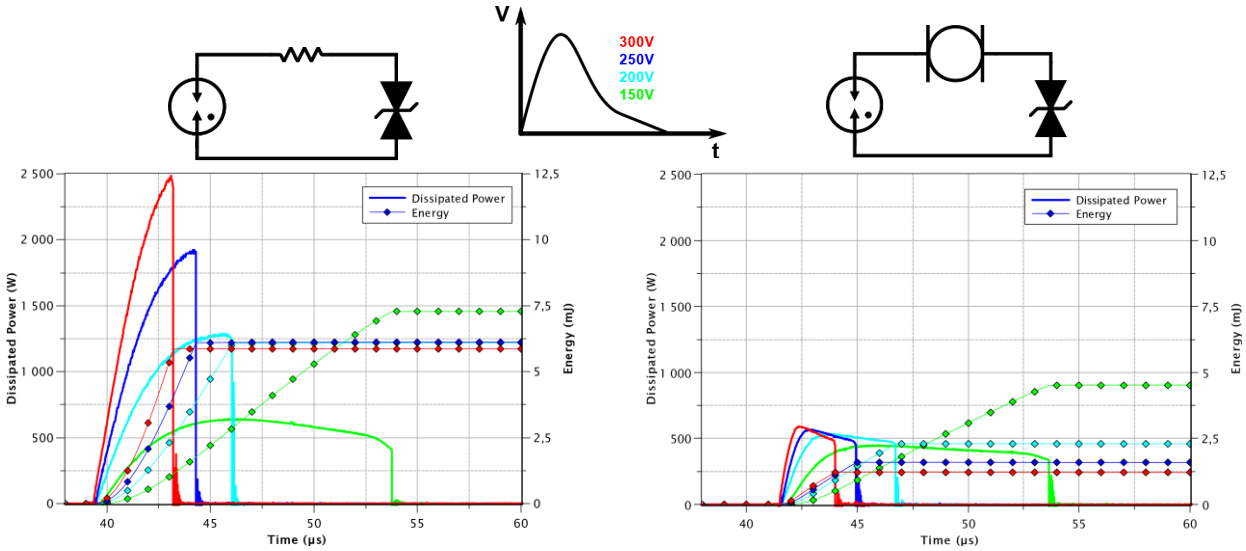

Figure 11: Waveforms showing power and energy dissipated by the TVS

Measured values for both solutions are summarized in the table below for a surge peak voltage of 300V.

@ 300V	I_{TVSmax} (A)	V_{TVSmax} (V)	P_{TVSmax} (W)	E_{TVSmax} (mJ)
With R	26	95	2470	6
With CLD	6.5	88	572	1.3

Table 1: Characteristic values for 300V surge

In Figure 10 (left), with resistor, it can be seen that the clamping voltage across the TVS continues to increase above its nominal voltage, before the GDT triggers; this is a consequence of not limiting the current during the transient. In addition, the dissipated power reaches high values, inducing thermal stress in the semiconductor, which can lead to a reduced TVS lifetime.

On the other hand, Figure 10 (right), the constant current behavior of the CLD enables a very sharp TVS voltage clamping. Moreover, the dissipated power is kept constant regardless the surge voltage, and maximum value is reduced by a factor of 4 compared to the resistor configuration (and even more if the input surge amplitude would be greater). This enables reducing the TVS power rating (size, cost, weight) when used in conjunction with a CLD.

An interesting side effect is the lowered dissipated energy as the input surge amplitude rises. This is related to the reduction of the GDT ignition time as the voltage amplitude (more precisely the dV/dt) increases. Since the dissipated power in the TVS is kept constant thanks to the CLD, the dissipated energy also decreases as the surge amplitude rises.

It can be noticed on Figure 10 that the GDT triggering voltage appears to be higher on the CLD-based circuit. This is expected because of the higher circuit input impedance. That way, before the GDT has triggered, the current drawn from the pulse generator is lower on the CLD-based circuit and, given the internal pulse generator impedance (2Ω), the generator output voltage is consequently higher. The same behavior would have occurred if a larger resistor value would have been used on the R-based circuit.

CONCLUSIONS

A new configuration of the π protection circuit using the CLD has been demonstrated in this Application Note, showing significant enhancements in the performance of this well-known circuit.

Compared to a resistor-based π protection circuit, the one using CLD offers lower insertion losses and an increased protection level. Indeed, by maintaining a low and constant dissipated power in the clamping voltage element (TVS), the clamping behavior is improved as well as reliability.

Additionally, TVS with smaller clamping voltage can be used. The use of smaller TVS (lower parasitics, size, cost, weight) also improves the frequency response of this circuit which is particularly attractive to protect interconnected communication systems against surges such as lightning.

The CLD-based π protection circuit can also efficiently protect current sensitive circuits such as trans-impedance amplifiers, current conveyors, 4-20mA sensor networks, etc…

Please contact CALY to request samples and test fixtures, and feel free to download the KE12LS200T electro-thermal SPICE model and its Application Note on CALY website to go deeper with the CLD.

REVISION HISTORY

Revision	Date	Description
1A	2017-Jun-13	First issue

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